In the claims:

Please amend claims 1, 3, and 4 as follows:

1. (Twice Amended) A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a first dielectric layer upon said oxide layer;

selectively removing said first dielectric layer to expose said oxide layer at a plurality of areas;

forming a second dielectric layer over said oxide layer and said first dielectric layer, wherein said forming a second dielectric layer includes forming a second dielectric layer over and in contact with the exposed oxide layer at said plurality of areas;

selectively removing said second dielectric layer to form a plurality of spacers from said second dielectric layer, wherein each said spacer is situated upon said oxide layer, is in contact with said first dielectric layer, and is adjacent to an area of said plurality of areas;

forming a plurality of isolation trenches extending below said oxide layer into said semiconductor substrate, wherein each said isolation trench is adjacent to and below a pair of said spacers and is situated at a corresponding area of said plurality of areas, and wherein each isolation trench has a top edge;

forming a liner upon a sidewall of each said isolation trench;

rounding the top edge of each of said isolation trenches;

filling each said isolation trench with a conformal layer, said conformal layer extending above said oxide layer in contact with a corresponding pair of said spacers,

wherein said filling is performed by depositing said conformal layer, and said depositing is carried out to the extent of leaving no gap in each said isolation trench and extending over said spacers and over said first dielectric layer; and

planarizing the conformal layer and each said spacer to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces, wherein said planarizing is performed in the absence of masking the conformal layer over the isolation trench;

wherein material that is electrically insulative extends continuously between and within said plurality of isolation trenches.

3. (Once Amended) A method according to Claim 1, wherein said a liner is a thermally grown oxide of said semiconductor substrate.

4. (Once Amended) A method according to Claim 1, wherein forming said liner upon said sidewall of said isolation trench comprises deposition of a composition of matter.